

What is claimed is:

- 1 1. A method for forming a wrap-around-gate field-effect transistor on a handle wafer,
2 comprising the steps of:
3 forming a silicon-on-insulator (SOI) structure on the handle wafer, the SOI structure
4 comprising a silicon island between a first oxide layer and a second oxide layer;
5 creating a first cavity in the SOI structure extending from a top surface of the SOI
6 structure to the handle wafer, the first cavity having substantially vertical sidewalls and
7 intersecting the silicon island;
8 isotropically etching the first oxide layer and the second oxide layer within the cavity
9 thereby exposing surface portions of the silicon island;
10 depositing on the surface portions a gate conductor material; and
11 isotropically etching the gate conductor material to form a wrap-around gate electrode
12 circumscribing a periphery of the silicon island.
- 1 2. The method of claim 1, further comprising the step of:
2 forming a gate dielectric on the surface portions.

1 3. A method for forming a wrap-around-gate field-effect transistor, comprising the steps of:
2 creating a first cavity in an SOI structure that intersects a semiconductor island
3 buried in oxide material;
4 etching the oxide material within the first cavity thereby exposing surface portions
5 of the semiconductor island;
6 depositing on the surface portions a gate conductor material;
7 etching the gate conductor material to form a wrap-around gate electrode that
8 encircles more than half of a periphery of the semiconductor island.

1 4. The method of claim 3, further comprising the step of:
2 forming a gate dielectric on the surface portions.

1 5. The method of claim 3, further comprising the step of:
2 forming an silicon-on-insulator (SOI) structure on a handle wafer.

1 6. The method of claim 3, wherein the first cavity includes substantially vertical sidewalls.

1 7. The method of claim 4, wherein the first cavity extends from a top surface of the SOI
2 structure to the handle wafer.

1 8. The method according to claim 3, wherein the oxide material comprises a first oxide
2 layer on the handle wafer below the semiconductor island and a second oxide layer above
3 the semiconductor island.

1 9. The method of claim 8, further comprising the step of:
2 forming a hard mask on the second oxide layer, the hard mask including an aperture
3 defining the first cavity.

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2 10. The method of claim 9, wherein the step of etching the first and second oxide layers is
3 performed anisotropically, using an aperture in the hard mask.

1 11. The method of claim 8, wherein the step of depositing further includes the steps of:
2 forming gate dielectric material on the surface portions;
3 depositing a conformal gate conductor material layer within the first cavity to cover
4 exposed portions of the first and second oxide layers and the silicon island; and
5 depositing an organic fill material to fill the first cavity.

1 12. The method of claim 11, further comprising the step of:
2 after depositing the organic fill material, directionally etching a second cavity based
3 on an aperture in the hard mask until at least a portion of the gate conductor material is
4 exposed within the second cavity.

1 13. The method of claim 12, wherein the second cavity includes substantially vertical
2 sidewalls.

- 1 14. The method of claim 12, further comprising the step of:
2 stripping the organic fill material from the second cavity.
- 1 15. The method of claim 9, further comprising the step of removing the hardmask.
- 1 16. The method according to claim 8, further comprising the step of:
2 removing the first and second oxide layers.
- 1 17. The method according to claim 3, further comprising the steps of:
2 forming source/drain regions on the semiconductor island; and
3 forming a first contact connected to the gate conductor material and a second contact
4 connected to the source/drain regions.
- 1 18. The method according to claim 3, further comprising the step of:
2 controlling a gate length of the wrap-around-gate field-effect-transistor by controlling
3 the etching of the oxide material and the gate conductor material.
- 1 19. The method according to claim 18, wherein the step of controlling includes the steps of:
2 anisotropically etching the oxide material a first distance from a vertical edge of the
3 first cavity;
4 isotropically etching the gate conductor material a second distance from the vertical
5 edge of the first cavity, the second distance being less than the first distance; and
6 wherein the gate length is substantially the difference between the first distance and
7 the second distance.

1 20. A portion of a wrap-around-gated field-effect transistor, the portion comprising:
2 an silicon-on-insulator (SOI) island comprising side surfaces forming a periphery and
3 extending, for a length, along a major axis in the horizontal direction; and
4 a gate electrode surrounding and supporting the SOI island, the gate electrode
5 extending in a vertical direction from a handle wafer and having a thickness, in the horizontal
6 direction, less than the length of the SOI island such that a portion of the SOI island extends
7 on one side of the gate electrode and another portion of the SOI island extends on another
8 side of the gate electrode, the gate electrode comprising:
9 a first portion below the SOI island, a second portion on one side of the SOI
10 island, and a third portion above the SOI island such that the gate electrode extends more
11 than half-way around the periphery of the SOI island.

1 21. The portion according to claim 20, wherein a first edge face of the SOI island extends
2 outward on one side of the gate electrode and a second edge face of the SOI island extends
3 oppositely outward on another side of the gate electrode.

1 22. The portion according to claim 20, wherein the gate electrode has a cross-sectional
2 profile that is C-shaped.

1 23. The portion according to claim 20, wherein a portion of a top surface of the SOI island
2 is exposed.

1 24. The portion according to claim 20, wherein at least a portion of the SOI island is
2 supported underneath by an oxide layer on the handle wafer.

- 1 25. A field-effect-transistor comprising:
2 a silicon-on-insulator (SOI) island comprising a surface periphery and two edge faces,
3 the SOI island oriented substantially in a horizontal direction;
4 a wrap-around gate electrode oriented in substantially a vertical direction intersecting
5 with the SOI island in-between the two edge faces such that the SOI island, such that the
6 wrap-around gate electrode extends more than half-way around the surface periphery of the
7 SOI island;
8 a source region formed on a first part of the SOI island, on one side of the gate
9 electrode; and
10 a drain region formed on a second part of the SOI island, on another side of the gate
11 electrode.
- 1 26. The field-effect transistor of claim 25, wherein a portion of a bottom surface of the SOI
2 island on both sides of the gate electrode is exposed.
- 1 27. The field-effect transistor of claim 25, wherein at least a portion of the SOI island is
2 supported underneath by an oxide layer.
- 1 28. The field-effect transistor of claim 25, wherein the wrap-around gate electrode extends
2 entirely around the surface periphery of the SOI island.